CLAIMS

What is claimed is:

1. A method of grouping cells in an integrated circuit design comprising steps of:

(a) receiving as input a representation of an integrated circuit design;

(b) initializing a corresponding list of cells for a common signal domain in the integrated circuit design;

(c) selecting a cell belonging to a common signal domain that is not included in a corresponding list of cells for a common signal domain;

(d) tracing a net from an input port of the selected cell to a signal driver and inserting the selected cell in the corresponding list of cells for the common signal domain associated with the signal driver; and

(e) tracing the net to an input port of each cell connected to the signal driver and inserting each cell traced from the net in the corresponding list of cells for the common signal domain associated with the signal driver.

2. The method of Claim 1 further comprising a step (f) of repeating steps (c), (d) and (e) until every cell belonging a common signal domain has been inserted in a corresponding list of cells for the common signal domain.

3. The method of Claim 2 further comprising a step (g) of generating as output a corresponding list of cells for a common signal domain in the integrated circuit design.

4. The method of Claim 1 wherein step (d) includes storing a name of the selected cell in the corresponding list of cells for the common signal domain associated with the signal driver.

5. The method of Claim 1 comprising performing steps (b), (c), (d) and (e) for cells that are flip-flops in a scan chain.

6. The method of Claim 5 comprising performing steps (b), (c), (d) and (e) for a common signal domain that is a scan clock domain.

7. The method of Claim 6 comprising performing steps (d) and (e) for a net that is a clock net.

8. The method of Claim 7 comprising performing steps (d) and (e) for an input port that is a clock port.

9. The method of Claim 8 comprising performing steps (d) and (e) for a signal driver that is a clock driver.

10. A computer program product for grouping scan flops for scan testing comprising:

a medium for embodying a computer program for input to a computer; and

a computer program embodied in the medium for causing the computer to perform steps of:

(a) receiving as input a representation of an integrated circuit design;

(b) initializing a corresponding list of cells for a common signal domain in the integrated circuit design;

(c) selecting a cell belonging to a common signal domain that is not included in a corresponding list of cells for a common signal domain;

(d) tracing a net from an input port of the selected cell to a signal driver and inserting the selected cell in the corresponding list of cells for the common signal domain associated with the signal driver; and

(e) tracing the net to an input port of each cell connected to the signal driver and inserting each cell traced from the net in the corresponding list of cells for the common signal domain associated with the signal driver.

11. The computer program product of Claim 10 further comprising a step (f) of repeating steps (c), (d) and (e) until every cell belonging a common signal domain has been inserted in a corresponding list of cells for the common signal domain.

12. The computer program product of Claim 11 further comprising a step (g) of generating as output a corresponding list of cells for a common signal domain in the integrated circuit design.

13. The computer program product of Claim 10 wherein step (d) includes storing a name of the selected cell in the corresponding list of cells for the common signal domain associated with the signal driver.

14. The computer program product of Claim 10 comprising performing steps (b), (c), (d) and (e) for cells that are flip-flops in a scan chain.

15. The computer program product of Claim 14 comprising performing steps (b), (c), (d) and (e) for a common signal domain that is a scan clock domain.

16. The computer program product of Claim 15 comprising performing steps (d) and (e) for a net that is a clock net.

17. The computer program product of Claim 16 comprising performing steps (d) and (e) for an input port that is a clock port.

18. The computer program product of Claim 17 comprising performing steps (d) and (e) for a signal driver that is a clock driver.